Digital Electronics.

CHAPTER THIRTY THREE

Semiconductor Random-Access Memories

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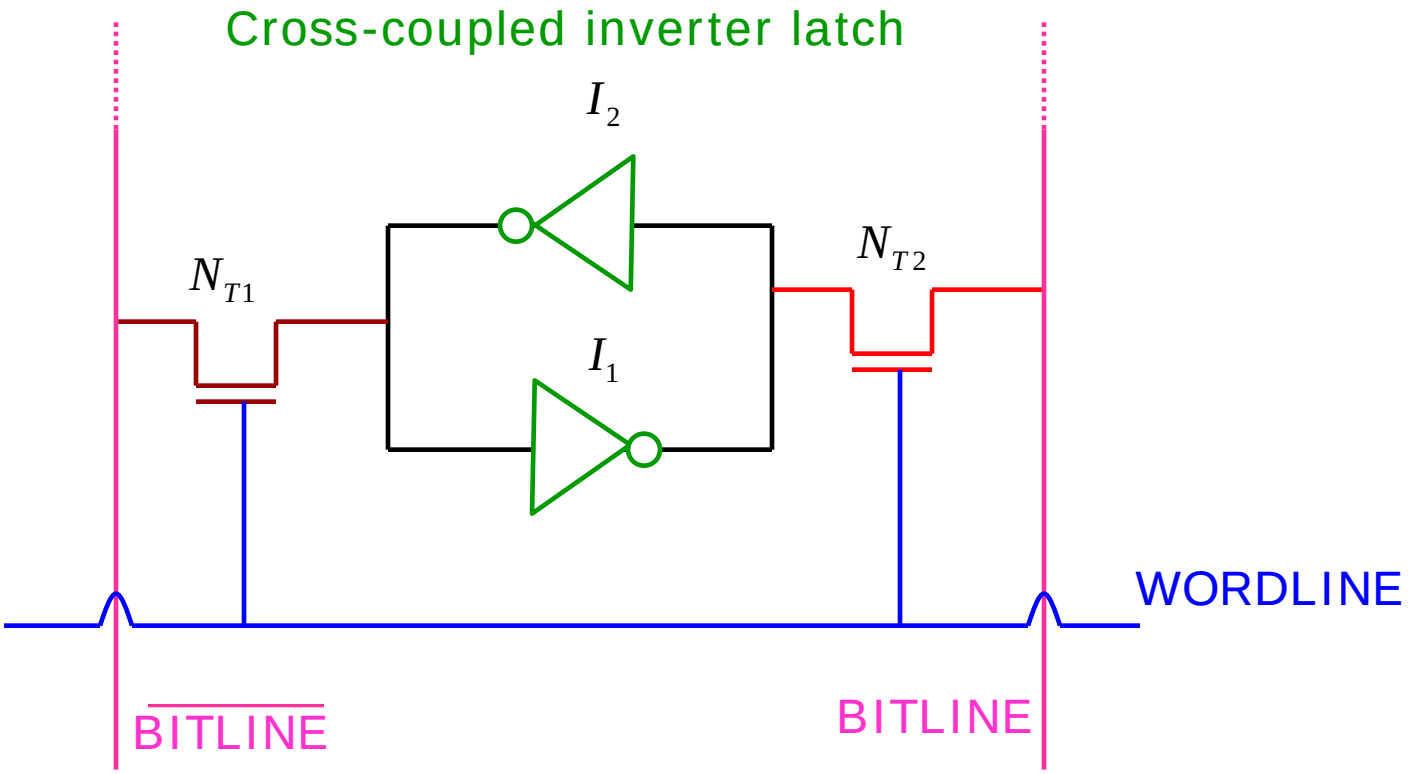
Introduction

In Random-Access Memories (RAM) the data can both be read (*independent of the order in which it was originally written*) and written after fabrication.

1. Static RAM (SRAM) (*in this chapter*): The data can be stored as long as power of semiconductor circuit remains uninterrupted. (faster →CPU cashes, less dense→ not for PC memory

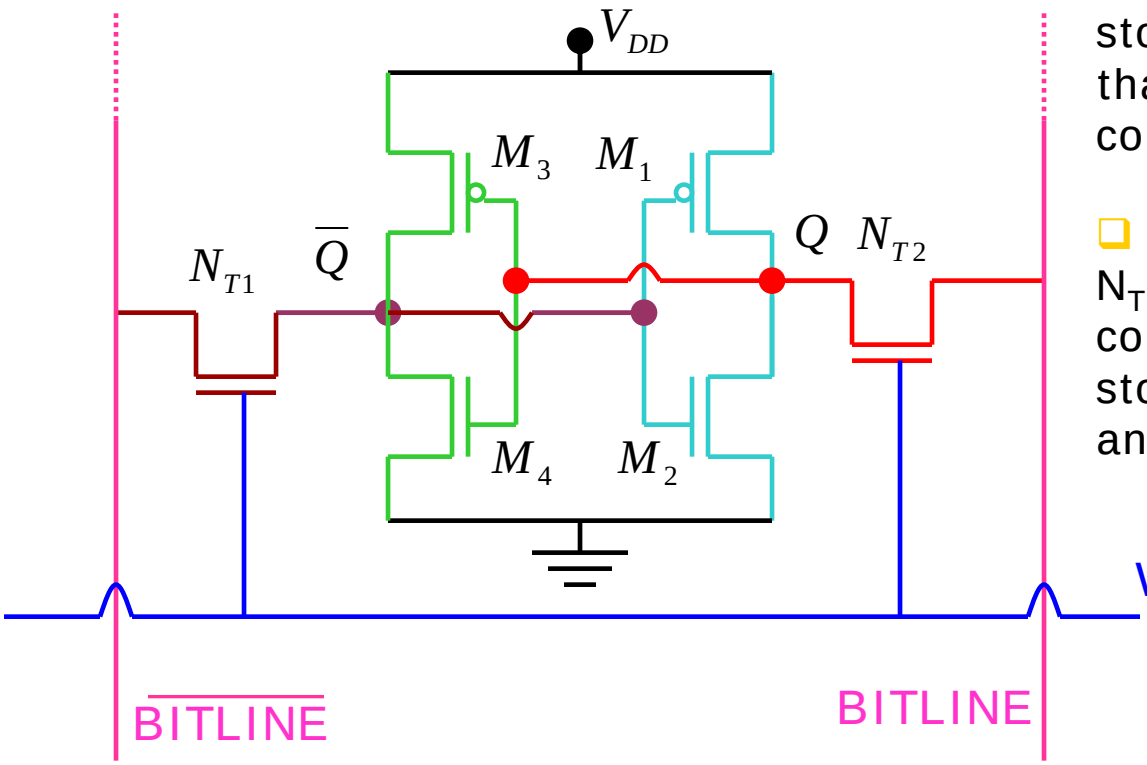
2. Dynamic RAM (DRAM): The data can be stored for several milliseconds by incorporating of active refreshing circuitry.

Static RAM Cell with Transmission Gates



Static RAM Cell with Transmission Gates

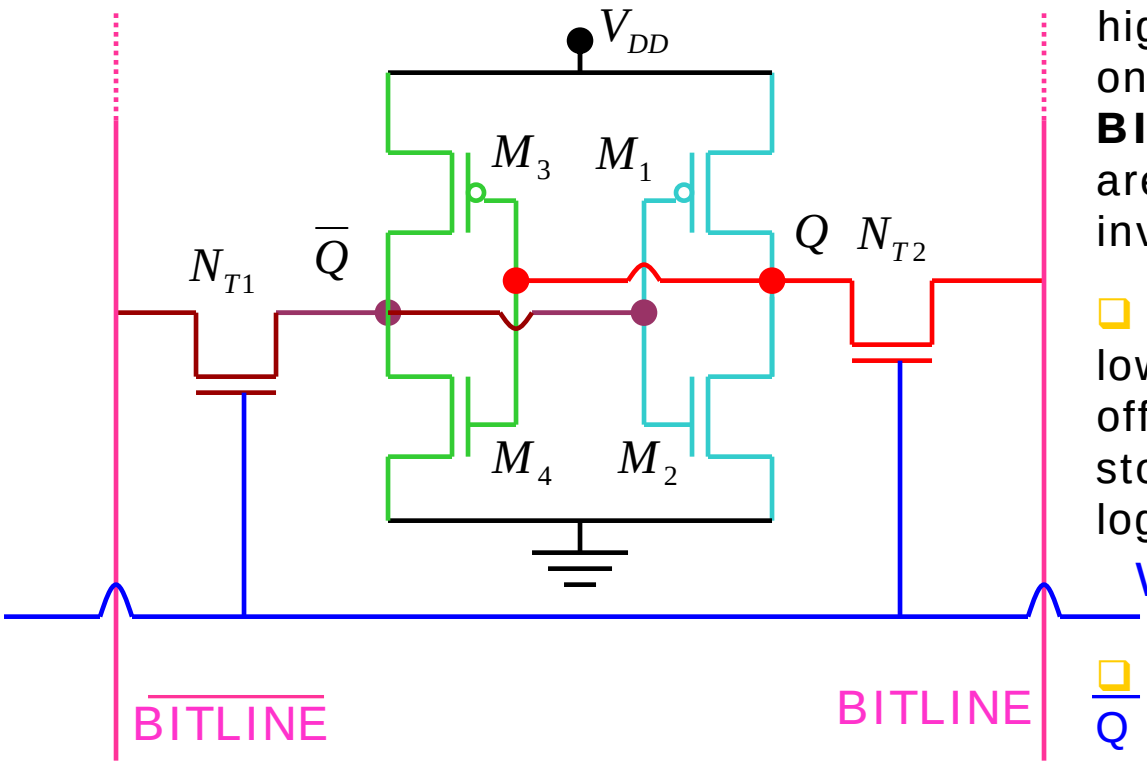
Cross-coupled inverter latch



- Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters
- The *access* transistors N_{T1} and N_{T2} serve to control the access to a storage cell during read and write operations

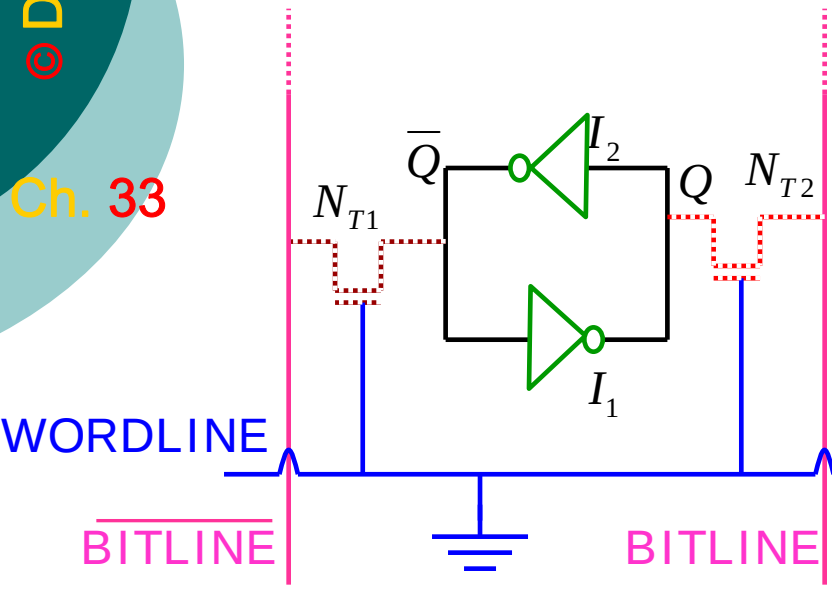
Static RAM Cell with Transmission Gates

Cross-coupled inverter latch



- When **WORDLINE** is high, both N_{T1} & N_{T2} are on, and then the lines **BITLINE** and **BITLINE** are connected to the inverters
- When **WORDLINE** is low, both N_{T1} & N_{T2} are off, and then RAM bit stores a stable binary logic level **0** or **1**
- For Q high→ M4 on→ $\overline{Q}$ is low→M2 off & M1 on
- For Q low→ M3 on→ $\overline{Q}$ is high→M2 on & M1 off

Storage of Single-Bit Data



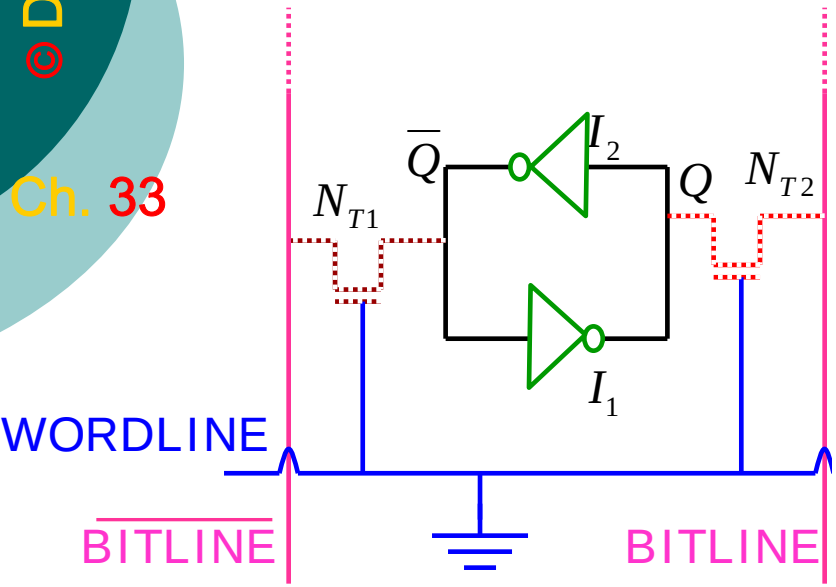
- For Q and $\overline{Q}$ are logic complements
- Q represents the state of the memory cell

Storage of a logic 1

- When the **WORDLINE** is grounded, the transmission NMOS devices are cut-off
- If the state Q is at logic **1**, then node at the output of the inverter I_2 is at logic **0,** this state represents **Q=1**.

① ***SRAM is in Standby operation***

Storage of Single-Bit Data

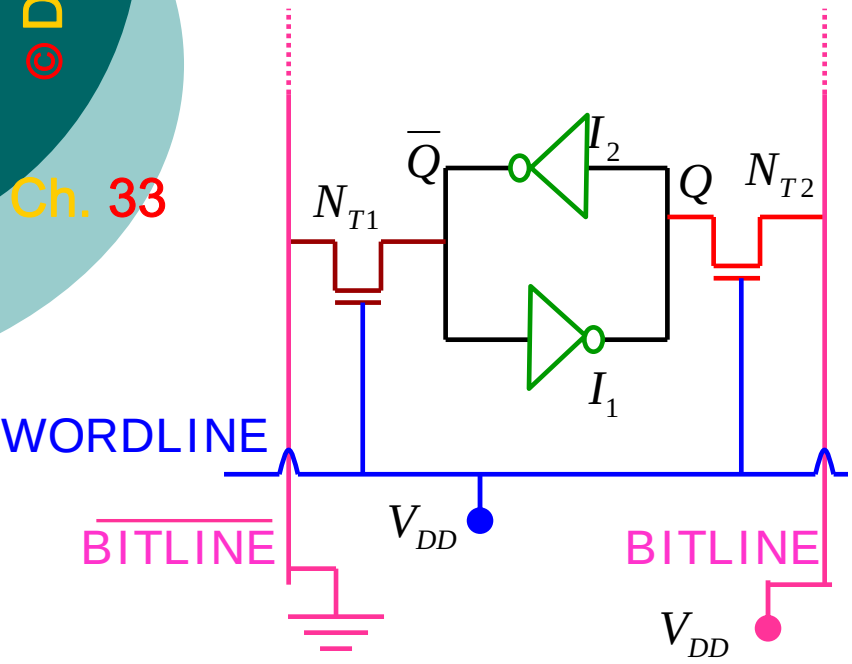


Storage of a logic 0

- When the **WORDLINE** is grounded, the transmission NMOS devices are cut-off
- If the state Q is at logic **0**, then node at the output of the inverter I_2 is at logic **1,** this state represents **Q=0**.

① ***SRAM is in Standby operation***

Writing to a Single-Bit



Writing of a logic 1

- When the **WORDLINE** is high, and the BITLINE is held high whereas **BITLINE** is held low, a logic **1** is written into the SRAM bit cell; i.e. the voltage levels of **BITLINE** and **BITLINE** are transmitted through the transmission MOSFETs to **Q** and **Q** nodes.

- Regardless of the logic level stored in the SRAM bit before the **WORDLINE** is high, the inverters switch to the values of **BITLINE** and **BITLINE**.

② ***SRAM is in writing operation***

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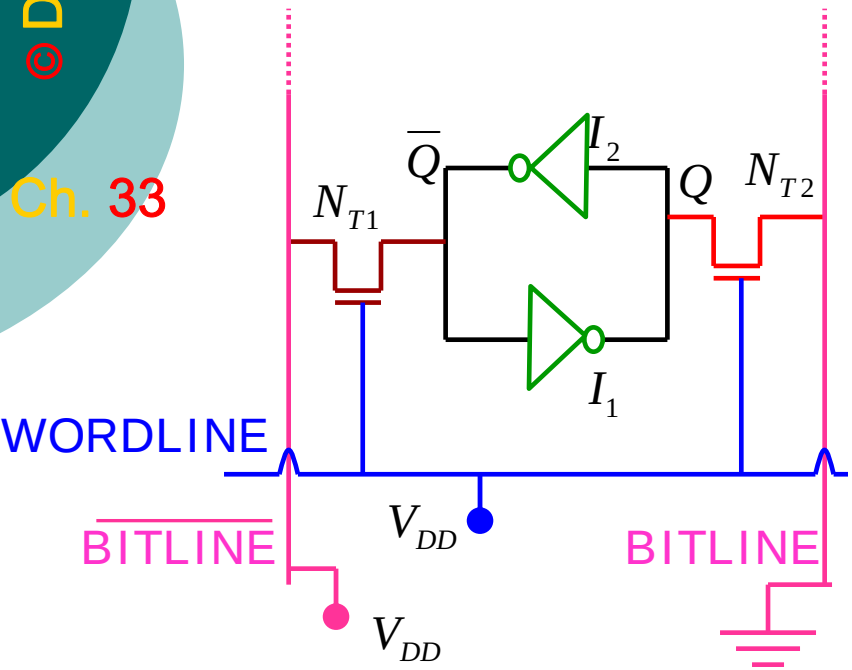
Writing to a Single-Bit



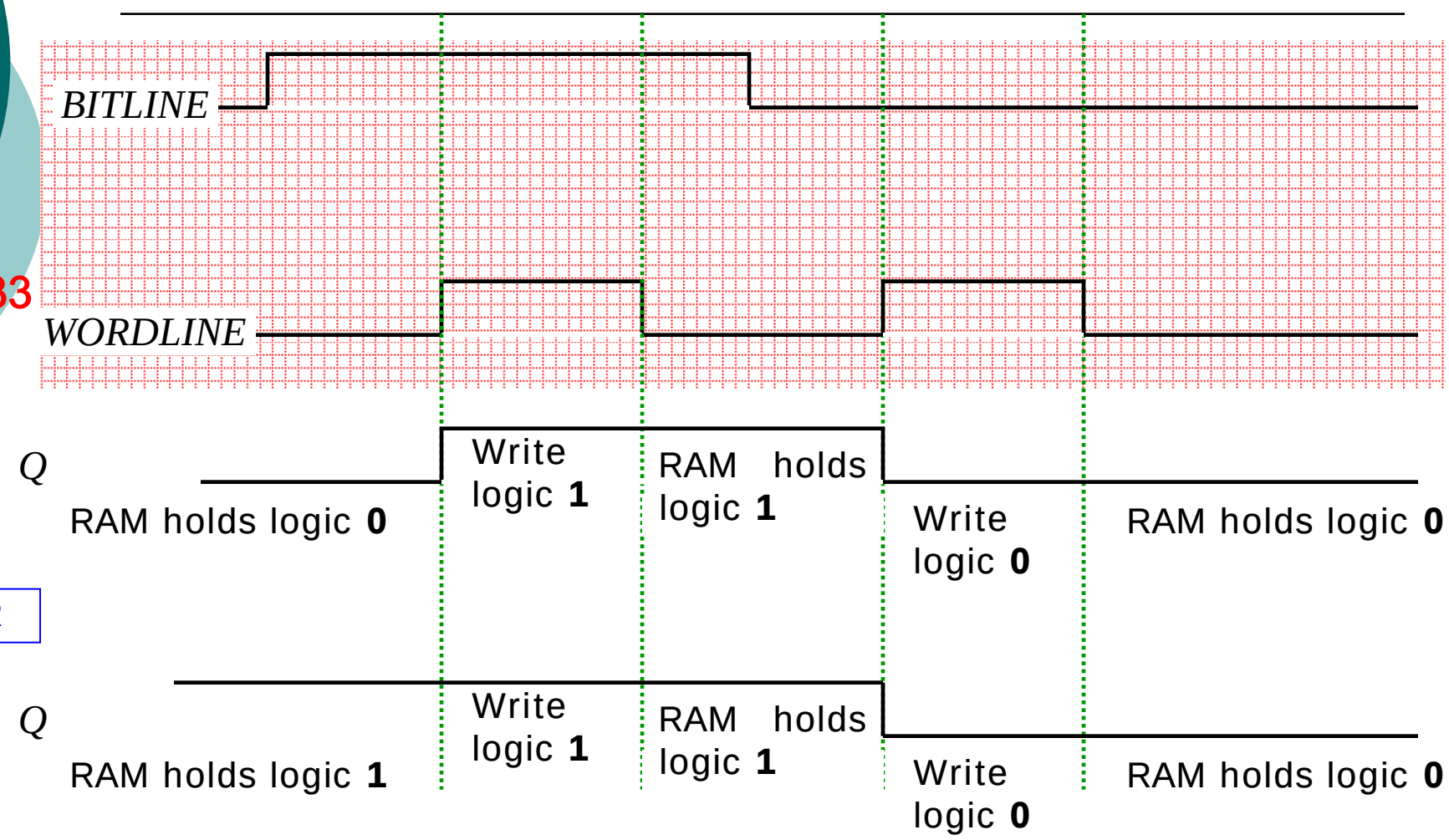
Writing of a logic 0

- When the **WORDLINE** is high, and the BITLINE is held low whereas **BITLINE** is held high, a logic **0** is written into the SRAM bit cell; i.e. the voltage levels of **BITLINE** and **BITLINE** are transmitted through the transmission MOSFETs to **Q** and **Q** nodes.

- Regardless of the logic level stored in the SRAM bit before the **WORDLINE** is high, the inverters switch to the values of **BITLINE** and **BITLINE**.

② ***SRAM is in writing operation***

Waveforms of Writing Logic 1s and 0s



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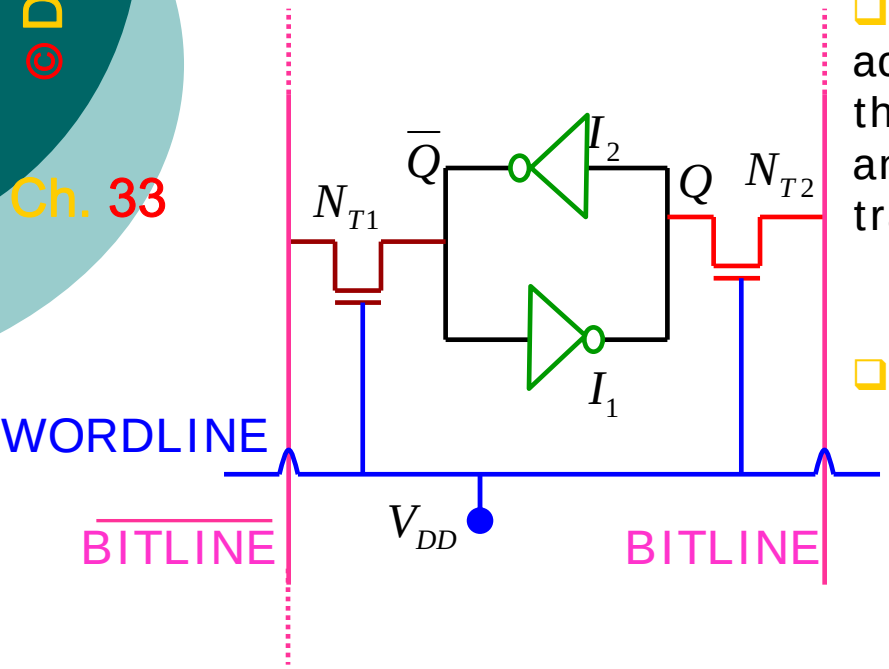
Reading from a Single-Bit



- Reading binary values from SRAM cell is accomplished by bringing the **WORDLINE** to the high state, and then driving the **BITLINE** and the **BITLINE** to the enabled NMOS transmission gates.

- **BITLINE = Q** and the $\overline{\textbf{BITLINE}}$**=**$\overline{\textbf{Q}}$

③ ***SRAM is in reading operation***